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References cited for evaluating patentability:
DE 197 28 692 A1
JP 1-27251 A – in: Patent Abstracts of Japan, Sect. E. Vol. 13 (1989) No. 216 (E-760)

Circuit configuration for interference suppression of integrated circuits

A low-inductance capacitor (12) is integrated into the housing (3) of a microchip (4). The capacitance connections (10, 11) of the low-inductance capacitor (12) are radially connected on the one hand via bond wires (5) with the ground and supply voltage bond points (1, 2) of the microchip (4) and on the other hand via additional bond wires (13) with at least one supply voltage pin pair (6, 7). At least one reference potential connection (14) of the low inductance capacitor (12) is electrically conductively connected with a floating ground (16).

Description

The invention relates to a circuit configuration for interference suppression of integrated circuits.

Increasing performance requirements of modern electronic systems, e.g. control devices, require increasingly more powerful integrated circuits (ICs). The computing capacity of microcomputers is constantly being increased by continuously reducing the chip structures, introducing new semiconductor technologies and increasing the system clock frequencies. On the other hand, the very fast pulse rise and fall times of these microcomputers generate narrowband interference signals, e.g. in the frequency range of between 30 MHz and 1 GHz, which are emitted through the power supply wiring of the microcomputer, among other things. Modern microcomputers thus represent a significant source of interference for surrounding electronic components, particularly radio receivers.

To meet today's high EMC requirements of electronic systems, effective and reliable interference suppression of IC components is indispensable. For interference suppression of microcomputers, it is known in the art to separate the voltage supply of the individual function blocks, e.g. CPU, clock generator and memory, and to provide several supply voltage connections with smoothing capacitors (block capacitors) connected in parallel on the microcomputer. Furthermore, metal housings, referred to as tuner boxes, additional input/output filters, and printed circuit boards with multilayer design are provided to ensure sufficient interference suppression. Such interference measures are described in the publication by W. Grözinger, "Elektromagnetische Verträglichkeit von integrierten Schaltkreisen" [Electromagnetic Compatibility of Integrated Circuits], VDI Berichte No. 1152, 1994, pp. 441 to 465. Despite these very costly measures, this type interference suppression of microcomputers occasionally fails to meet EMC requirements.

An integrated circuit, e.g. a microcomputer, has many individual internal interference sources, e.g. clock generator or CPU. The emission behavior thereby decisively depends on the rise and fall rates of the supply current, i.e. the greater the edge steepness dI/dt, the greater the noise emission. To prevent the latter from being distributed via the supply wiring over the entire printed circuit board and ultimately over the entire electronic system, a block capacitor, which acts as an energy reserve for fast current requirements, is typically connected in parallel to each supply voltage pin pair on the IC housing.

The effect of this block capacitor thereby substantially depends on its self-inductance and the connection inductances. The lower the inductive component is, the better is the efficiency of the block capacitor in the higher frequency ranges. Since the inductive component, however, cannot be reduced at will due to technical limitations – known configurations fall within the range of 10 nH – fast energy requirements in such a configuration are not only covered by the block capacitor but are also supplied via large-area and thus low-impedance reverse current paths (grounds) partly from the power supply, so that an interference signal is distributed over the entire electronic system.

DE 197 28 692 A1 describes an IC chip in which one or several electronic components are accommodated within the housing in the immediate vicinity of the integrated circuit. By

relocating components that are normally provided outside the IC chip to the interior of the chip, the IC chip can be used even at the highest frequencies and operating speeds.

Furthermore, from JP 1-27251 A in: Patent Abstracts of Japan, Sect. E. Vol. 13 (1989) No. 216 (E-760), it is known to provide a capacitor on the substrate element of a microchip and thus to decrease inductance and reduce interference signals.

The object of the invention is to develop a circuit configuration that ensures reliable interference suppression of integrated circuits.

This object is attained according to the invention by a circuit configuration with the features of Claim 1. Advantageous further developments of the invention are set forth in the subclaims.

Capacitance networks, e.g. Syfer's X2Y 3 terminal capacitor, are known in the art today and due to their special symmetrical structure and the mutual cancellation of the magnetic fields connected therewith, have very low self-inductance – in the range of 50 pH. Such capacitance networks are hereinafter generally referred to as low inductance capacitors. According to the invention, such a low-inductance capacitor is integrated in the housing of an IC, and all power supply bond points of the microchip are radially connected via bond wires with the low-inductance capacitor. This arrangement within the IC housing also causes the connection inductance to be significantly reduced compared to conventional structures. The low-inductance capacitor then provides the energy that is quickly required by various function blocks immediately on the microchip within the requisite time. On the outside of the housing, only a voltage supply pin pair is required to connect the supply leads. This pin pair is also connected to the low-inductance capacitor via bond wires. Thus all the other previously used supply voltage pins on the IC housing are available for other functions. No additional smoothing capacitors are required, which saves a substantial amount of space on the printed circuit board. The heretofore unequaled low inductance connection of the energy reserve for fast current requirements reduces the interference voltages to the point where additional interference suppression measures, e.g. the use of multilayer printed circuit boards, can frequently be dispensed with.

An exemplary embodiment of the invention will now be described by means of the figures in which:

Fig. 1 is a schematic representation of a prior art circuit configuration for interference suppression of an integrated circuit and

Fig. 2 is a schematic representation of a circuit configuration according to the invention for interference suppression of an integrated circuit.

To provide a better understanding of the invention, a prior art circuit configuration for interference suppression of an integrated circuit with separate voltage supply will now be described by means of Fig. 1. Supply voltage bond points 1 and ground bond points 2 of a microchip 4 arranged in an IC housing 3 are connected via bond wires 5 with the supply voltage connections 6 and the ground connections 7 brought out of the IC housing. This makes it possible to supply different function blocks of microchip 4 with a voltage separately from each other and thus to reduce the interference emission of the IC. However, fast current requirements of individual function blocks and the edge steepness (dI/dt) connected therewith nevertheless result in high frequency interference voltages that with direct supply from a power supply (not

depicted) are distributed over the entire electronic system, e.g. a control device, via the low-impedance ground leads. This is why a block capacitor 8 is connected in parallel to each terminal pair 6, 7 to act as an energy reserve for currents that are quickly required by the corresponding function block.

A circuit configuration according to the invention is depicted in Fig. 2. Components that coincide with the parts shown in Fig. 1 carry identical reference numbers. The supply voltage bond points 1 and the ground bond points 2 of microchip 4 are radially connected via bond wires 5 with capacitance connections 10 and 11 of a low-inductance capacitor 12.

Radially in this case means that all supply voltage bond points 1 are connected with the one connection, e.g., capacitance connection 10, and all ground bond points 2 are connected with the other connection, e.g. capacitance connection 11. Via additional bond wires 13, capacitance connections 10 and 11 of the low inductance capacitor 12 are connected with a supply voltage pin pair 6, 7 brought out of IC housing 3. Capacitance connection 10 connected with supply voltage bond points 1 is thereby connected to supply voltage connection 6, and capacitance connection 11 connected with ground bond points 2 is connected to ground connection 7. At least one, but preferably two, reference potential connections 14 of capacitance network 12 are electrically conductively connected with a floating ground 16 which has no galvanic connection to the ground leads serving as reverse current path.

Since the low inductance capacitor 12 integrated in IC housing 3 already provides the energy for the fast current requirements of all functional units on microchip 4, no external block capacitors are required. Additional connections 6 and 7 that heretofore served for separate voltage supply of the individual function blocks are no longer required and can thus be used for other functions. If a supply voltage connection on IC housing 3 should not be sufficient to meet the current demand from the power supply in normal operation, i.e. with non-critical edge steepness of the current pulses, additional pin pairs 6, 7 can be connected via bond wires 13 to the low inductance capacitor 12.

Low inductance capacitor 12 is preferably constructed in thin film technology on a ceramic substrate, but can also be realized monolithically on a silicon chip.

The invention was described by way of example based on the figures for an integrated circuit with two separate supply voltage pin pairs, but it is also suitable for a higher number of supply voltage pin pairs as well as for integrated circuits that have no separate voltage supply.

Claims

1. Circuit configuration for interference suppression of integrated circuits with
   - a microchip (4) arranged in an IC housing (3),
   - at least one supply voltage bond point (1) on micro chip (4) for connection to a supply voltage,
   - at least one ground bond point (2) on microchip (4) for connection to a ground potential,

- at least one supply voltage pin pair (6, 7) brought out of the IC housing (3), comprising a supply voltage connection (6) and a ground connection (7) to connect a supply lead or a ground lead, and
- a low inductance capacitor (12) integrated in the IC housing (3), having
  - capacitance connections (10, 11) each radially connected via bond wires (5) with the supply voltage bond point (1) and ground bond point (1, 2) of the microchip (4), and via additional bond wires (13) with at least one supply voltage pin pair (6, 7), and
  - at least one reference potential connection (14) electrically conductively connected with a floating ground (16).

2. Circuit configuration as claimed in Claim 1, characterized in that the low inductance capacitor (12) is realized monolithically on a silicon chip.

2 pages of drawings

DRAWINGS PAGE 1

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FIG. 1

St. d. T. = prior art